CLAIMS

1. (Cancelled) A method of conserving power in a CPU (processor unit), comprising the steps of:

providing upper and lower bit data register circuitry portions where both upper and lower portions are active when both are simultaneously useable with presently active software operating in said CPU;

detecting the machine state occurring because of presently running software; and

supplying voltage and clocks to only lower bit data register circuitry in accordance the machine state detection that the presently operating software can actively use only said lower bit data register circuitry portions.

2. (Cancelled) A method for controlling voltage and clocks in a microprocessor, comprising:

generating architected bits in a machine state register associated with at least one function to be enabled or disabled in said microprocessor; and

utilizing said bits to enable or disable said at least one function.

3. (Cancelled) Computer apparatus, comprising:

register circuitry segregated into a plurality of sectional parts, each with separate power control mechanisms;

register state detection means operable to provide at least one signal indicative of the instruction set width of software operatively running on said computer apparatus; and power shutdown means, responsive to said at least one signal, operating to remove at least one of voltage and clocks from sectional parts of said register circuitry that would not be actively used by the software presently operating in said computer apparatus.

4. (Cancelled) The apparatus of claim 3 wherein the sectionalized registers are utilized for dataflow.

5. (Cancelled) A method of conserving power in a CPU (processor unit), comprising:

constructing data flow circuitry into a plurality of sections, at least one of which can be controllably activated;

detecting the machine state; and

providing voltage to sections of said data flow circuitry as a function of the machine state detected.

6. (Cancelled) A method of conserving power in a CPU (processor unit), having a software accessible control register and further having sectionalized data transfer registers, comprising:

detecting the machine state as determined by the control register; and

activating sectional portions of the data transfer registers as a function of the detected machine state.

7. (Cancelled) A method of conserving power in a CPU (processor unit), having a software accessible control register and further having specialized computational sections, comprising:

detecting the machine state as determined by the control register; and

activating specialized computational portions of the CPU as a function of the detected machine state.

8. (Cancelled) A method of conserving power in a CPU (processor unit), having a software accessible control register and further having sectionalized clock signal distribution means, comprising:

detecting the machine state as determined by the control register; and

activating sectionalized portions of the clock signal distribution means as a function of the detected machine state.

9. (Cancelled) A method of conserving power in a CPU (processor unit), having a software accessible control register, comprising:

detecting the machine state as determined by the control register; and

de-activating at least one of,

(a) sectionalized portions of a clock signal distribution means as a function of the detected machine state,

(b) sectional portions of the data transfer registers as a function of the detected machine state, and

(c) floating point arithmetic unit,

as a function of the status of the control register.

10. (Cancelled) A method of conserving power in a CPU (processor unit), having a software accessible control register, comprising:

partitioning dataflow registers such that a lower portion register is consistent in size with the lowest instruction width software to be used in the CPU; and

using an architected control register bit whose logic level is indicative of the width of the greatest width software presently being used by the CPU to deactivate sectional portions of the dataflow registers that cannot be utilized by the presently loaded software.

11. (Cancelled) The method of claim 10 comprising, in addition:

partitioning arithmetic logic units (ALU) in the same manner as dataflow registers; and

using said architected control register bit to deactivate sectional portions of ALUs that cannot be utilized by the presently loaded software.

12. (Cancelled) The method of claim 10 comprising, in addition:

using an architected control register bit whose logic level is indicative of whether loaded software presently requires the use of a floating point logic unit (FPU) to activate the FPU only when software instructions are detected that require floating point logic.

13. (Cancelled) Apparatus for controlling power in a CPU (processor unit), comprising:

a software accessible machine state register having predetermined bit positions logically indicative of functions to be enabled or disabled in said CPU; and power activation means operating in accordance with the logic value of said predetermined bit positions to enable or disable said functions.

14. (Cancelled) A computer program product for conserving power in a CPU (processor unit), having a software accessible control register and further having sectionalized data transfer registers, the computer program product having a medium with a computer program embodied thereon, the computer comprising:

computer code for detecting the machine state as determined from the control register; and

computer code for activating sectional portions of the data transfer registers as a function of the detected machine state.

15. (Cancelled) A computer program product for conserving power in a CPU (processor unit), having a software accessible control register and further having specialized computational sections, the computer program product having a medium with a computer program embodied thereon, the computer comprising:

computer code for detecting the machine state as determined in the control register; and

computer code for activating specialized computational portions of the CPU as a function of the detected machine state.

16. (New) A method of conserving power in a computer processor, comprising:

reading a software-accessible control register;

determining an idle status of a subunit of the computer processor based on the control register;

providing a clock signal to the subunit based on the determined idle status; and

providing a power voltage to the subunit based on the determined idle status.

17. (New) The method as recited in Claim 16, wherein the control register comprises a plurality of architected bits in a machine state register and at least one bit of the plurality of architected bits is associated with at least one subunit of the computer processor.

18. (New) The method as recited in Claim 17, wherein determining the idle status comprises reading the at least one bit associated with the at least one subunit of the computer processor.

19. (New) The method as recited in Claim 16, further comprising setting one or more of a plurality of bits in the control register based on an idle status of a subunit of the computer processor.

20. (New) The method as recited in Claim 16, wherein the computer processor comprises data flow circuitry comprising a plurality of data flow sections, at least one data flow section configured as a subunit of the computer processor.

21. (New) The method as recited in Claim 16, wherein the computer processor comprises upper and lower bit data register circuitry portions, at least the upper bit data register circuitry portion configured as a subunit of the computer processor.

22. (New) The method as recited in Claim 16, wherein:

the computer processor comprises partitioned dataflow registers comprising a lower portion register consistent in size with the lowest instruction width software to be used in the computer processor; and

the control register comprises an architected control register bit indicating the width of the greatest instruction width presently being used by the computer processor.

23. (New) The method as recited in Claim 16, wherein the computer processor comprises partitioned arithmetic logic units (ALUs), comprising an upper ALU and a lower ALU, at least the upper ALU configured as a subunit of the computer processor.

24. (New) The method as recited in Claim 16, wherein the computer processor comprises a floating point logic unit (FPU), the FPU configured as a subunit of the computer processor.

25. (New) An apparatus for conserving power in a computer processor, comprising:

a software accessible control register having predetermined bit positions indicating subunits of the computer processor;

a local clock buffer coupled to the control register and configured to provide a clock signal to the subunit based on the predetermined bit position associated with the subunit; and

a voltage signal coupled to the control register and configured to provide a power voltage to the subunit based on the predetermined bit position associated with the subunit.

26. (New) The apparatus as recited in Claim 25, wherein the control register comprises a plurality of architected bits in a machine state register and at least one bit of the plurality of architected bits is associated with at least one subunit of the computer processor.

27. (New) The apparatus as recited in Claim 25, further comprising software configured to set one or more of the predetermined bit positions based on an idle status of a subunit of the computer processor.

28. (New) The apparatus as recited in Claim 25, wherein the computer processor comprises data flow circuitry comprising a plurality of data flow sections, at least one data flow section configured as a subunit of the computer processor.

29. (New) The apparatus as recited in Claim 25, wherein the computer processor comprises upper and lower bit data register circuitry portions, at least the upper bit data register circuitry portion configured as a subunit of the computer processor.

30. (New) The apparatus as recited in Claim 25, wherein:

the computer processor comprises partitioned dataflow registers comprising a lower portion register consistent in size with the lowest instruction width software to be used in the computer processor; and

the control register comprises an architected control register bit indicating the width of the greatest instruction width presently being used by the computer processor.

31. (New) The apparatus as recited in Claim 25, wherein the computer processor comprises partitioned arithmetic logic units (ALUs), comprising an upper ALU and a lower ALU, at least the upper ALU configured as a subunit of the computer processor.

32. (New) The apparatus as recited in Claim 25, wherein the computer processor comprises a floating point logic unit (FPU), the FPU configured as a subunit of the computer processor.

33. (New) A computer program product for conserving power in a computer processor, the computer program product having a medium with a computer program embodied thereon, the computer program comprising:

computer program code for reading a software-accessible control register;

computer program code for determining an idle status of a subunit of the computer processor based on the control register;

computer program code for providing a clock signal to the subunit based on the determined idle status; and

computer program code for providing a power voltage to the subunit based on the determined idle status.

34. (New) The computer program product as recited in Claim 33, wherein the control register comprises a plurality of architected bits in a machine state register and at least one bit of the plurality of architected bits is associated with at least one subunit of the computer processor.

35. (New) The computer program product as recited in Claim 34, wherein computer program code for determining the idle status comprises computer program code for reading the at least one bit associated with the at least one subunit of the computer processor.

36. (New) The computer program product as recited in Claim 33, further comprising computer program code for setting one or more of a plurality of bits in the control register based on an idle status of a subunit of the computer processor.